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14. ABSTRACT

The proposed STTR Phase I project objectives were to demonstrate the feasibility of high-frequency (HF) field-effect transistors (FETs) using novel 2-dimensional (2D) MoS2 semiconductor. Key components of the projects were:

1. Demonstrate large-area growth of mono and multi-layer MoS2 layers using chemical vapor deposition methods with great uniformity and reproducibility.

2. Fabricate large-periphery radio-frequency field-effect transistors which will employ conventional fabrication

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Report Title

Final Report: Two-Dimensional MoS2 Transistors for Low-Power RF Applications

ABSTRACT

The proposed STTR Phase I project objectives were to demonstrate the feasibility of high-frequency (HF) field-effect transistors (FETs) using novel 2-dimensional (2D) MoS2 semiconductor. Key components of the projects were:
1. Demonstrate large-area growth of mono and multi-layer MoS2 layers using chemical vapor deposition methods with great uniformity and reproducibility.
2. Fabricate large-periphery radio-frequency field effect transistors which will employ conventional fabrication methods using contact or projection lithography for high throughput device manufacturing.
3. Engineer source/drain contacts, gate dielectrics and develop novel concepts of "layer engineering" for high frequency operation.

Enter List of papers submitted or published that acknowledge ARO support from the start of the project to the date of this printing. List the papers, including journal references, in the following categories:

(a) Papers published in peer-reviewed journals (N/A for none)

Received Paper

TOTAL:

Number of Papers published in peer-reviewed journals:

(b) Papers published in non-peer-reviewed journals (N/A for none)

Received Paper

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Number of Presentations: 0.00

Non Peer-Reviewed Conference Proceeding publications (other than abstracts):

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Number of Non Peer-Reviewed Conference Proceeding publications (other than abstracts):

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Number of Peer-Reviewed Conference Proceeding publications (other than abstracts):

(d) Manuscripts

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Number of Manuscripts:

Books

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TOTAL:

Received Book Chapter

TOTAL:

Patents Submitted

Patents Awarded

Awards

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NAME	PERCENT_SUPPORTED	Discipline
Hao.	1.00	
FTE Equivalent:	**1.00**	
Total Number:	**1**	

Names of Post Doctorates

NAME	PERCENT_SUPPORTED
FTE Equivalent:	
Total Number:	

Names of Faculty Supported

NAME	PERCENT_SUPPORTED	National Academy Member
Prof. Qiliang Lee	0.30	
FTE Equivalent:	**0.30**	
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Names of other research staff

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Sub Contractors (DD882)

1 a. George Mason University

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Sub Contractor Numbers (c):
Patent Clause Number (d-1):
Patent Date (d-2):
Work Description (e):
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Sub Contract Est Completion Date(f-2):

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Scientific Progress

Technology Transfer

N5 Sensors, Inc.

Final Technical Report

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Dated: 03/16/2015

1. Project Objectives

The proposed STTR Phase I project objectives were to demonstrate the feasibility of high-frequency (HF) field-effect transistors (FETs) using novel 2-dimensional (2D) MoS_2 semiconductor. Key components of the projects were:

- **Demonstrate large-area growth of mono and multi-layer MoS_2 layers using chemical vapor deposition methods with great uniformity and reproducibility.**
- **Fabricate large-periphery radio-frequency field effect transistors which will employ conventional fabrication methods using contact or projection lithography for high throughput device manufacturing.**
- **Engineer source/drain contacts, gate dielectrics and develop novel concepts of "layer engineering" for high frequency operation.**

2. Description of the Research

Semiconducting 2D TMDs have shown unique properties due to their low dimension. Hence, they can utilized for next generation low-power electronics, particularly for high frequency RF transistors. These materials have greater flexibility than other 2D materials (e.g., graphene) and they can be easily grown or transferred on various substrates including the flexible ones to fabricate electronic and optoelectronic devices. Also, 2D materials have finite bandgap, hence they are suitable for low-power electronics, switching circuits with high on-off current ratio and metal-oxide-semiconductor FETs based electronics. Considering the potential of 2D materials, it is very important to develop a uniform growth strategy on various substrates over a large-area so that they can be viable for commercial device application. Simultaneously, exploring and understanding their electronic and optical properties are also very critical.

N5 Sensors, Inc. has demonstrated the feasibility of higher layer counts (3 – 4 layers) MoS_2 devices with clear advantages in terms of on-current, off-state leakage, noise figure, and transconductance. A new-concept of layer-engineering has been developed to understand the material properties and engineer the MoS_2 FETs to establish the high-frequency operations. In order to scale the growth process over a large area of 100 mm^2, N5 Sensors in collaboration with George Mason University (GMU), has built a chemical vapor deposition (CVD) reactor and established the feasibility of multilayer growth to fabricate RF transistors. In order to achieve low-contact resistance in those devices, high-performance highly-stable contacts have been engineered to achieve low specific resistance.

During the period of performance, we completed several growth runs with iterative optimization, conducted material characterization (Raman scans, photoluminescence, hall mobility measurements). We established fabrication processes, optimized metal contact stacks and annealing conditions, developed and optimized etching recipes, demonstrated large-area devices using standard microfabrication process and reported dc characterization of the transistors.

3. Works performed and Results

In order to achieve the project objectives, the following tasks were performed in this project and the results are also summarized.

Task 1: Demonstration of High-Quality Large-Area MoS_2 Layers

Subtask 1.1 Growth of 10 x 10 mm^2 monolayer and multilayer MoS2 on device-quality substrates

N5 has collaborated with Prof. Qiliang Li from GMU to develop a novel technique for high-quality large-area (10 x 10 mm^2) growth of MoS_2. Chemical vapor deposition (CVD) method has been employed to grow MoS_2 layers with monolayer-control on various substrates for device integration. Typical setup for the CVD reactor is shown in Fig. 1 (left) in which MoS_2 semiconductor with mono- and multilayers is grown by sulfurization of thin layers of ebeam-deposited Mo film. Figure 2 (right) shows the growth obtained on quartz substrates with various initial layer thicknesses.

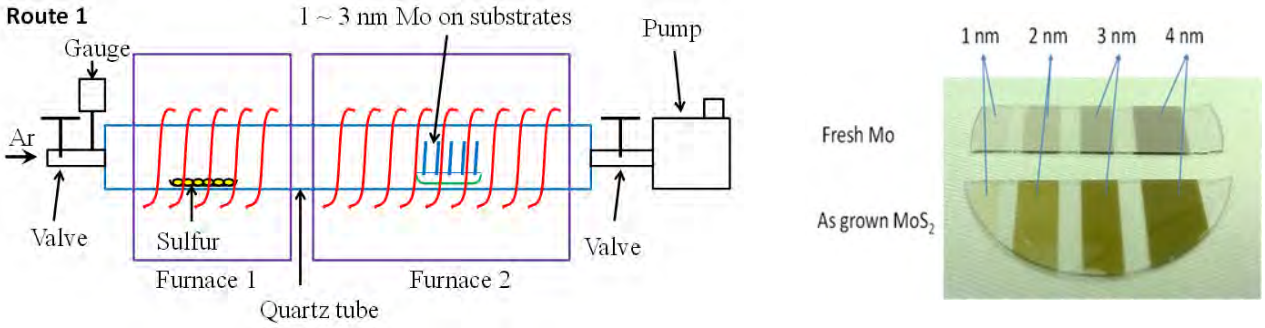

Figure 1. (Left) The schematic of CVD reactor in which MoS_2 monolayer or few-layers are grown. **(Right)** Fresh Mo and sulfurized MoS_2 films on quartz substrate showing various thicknesses.

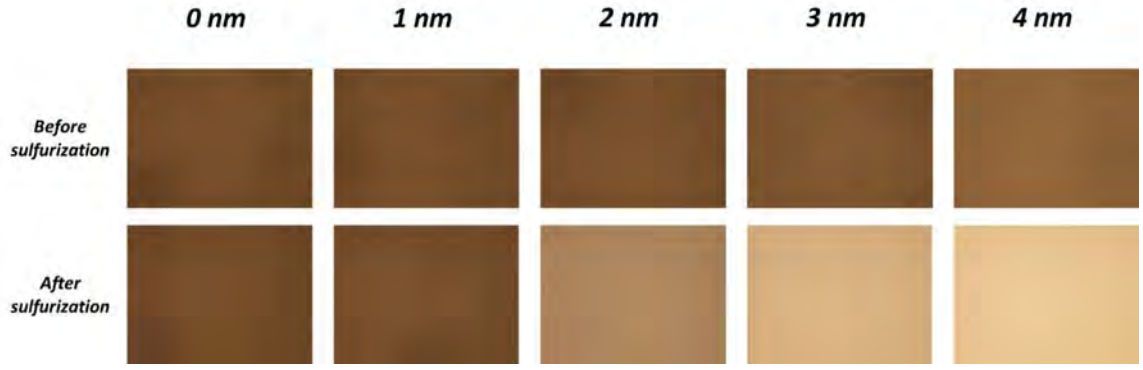

Figure 2. Optical micrographs showing the samples before and after sulfurization at 750 ºC for 10 min.

The CVD process has been further optimized to achieve 10 x 10 mm^2 unifrom growth. Firstly, metal Mo was deposited by e-beam evaporation, subsequently loaded to the CVD chamber. The deposition rate is ~0.1 Å/s for Mo. The sulfurization was carried out in a horizontal tube furnace, with the S source at the upstream load, Mo samples at the center zone and Ar as carrier gas with flow rate of 150 - 200 sccm. The furnace was heated up to 500 ^oC in 30 min, then heated up to 750 ^oC in 60 min, and kept at 750 ^oC for 10 min before the substrates were cooled down naturally. The temperature at S source was kept at ~140 ^oC during deposition. The optical micrsocope image of the samples with different Mo and after sulphurization is shown in Fig. 2.

Subtask 1.2 Spectroscopic characterization

In order to evaluate the uniformity of MoS2 over the large area, Raman spectroscopy has been used. Typical Raman spectra of MoS_2 samples with different Mo thicknesses are shown in Fig. 3.

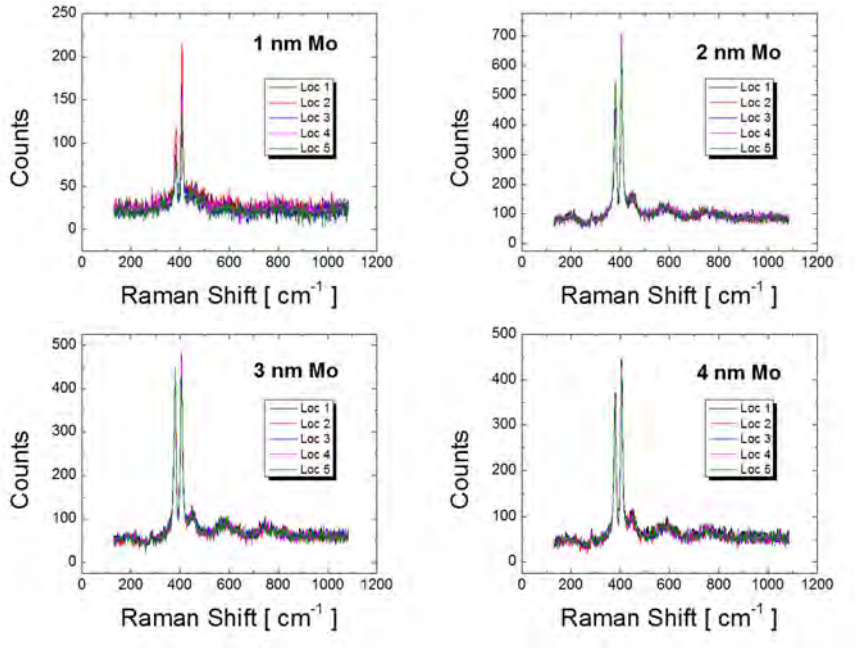

Figure 3. Typical Raman spectra of MoS_2 films at different locations.

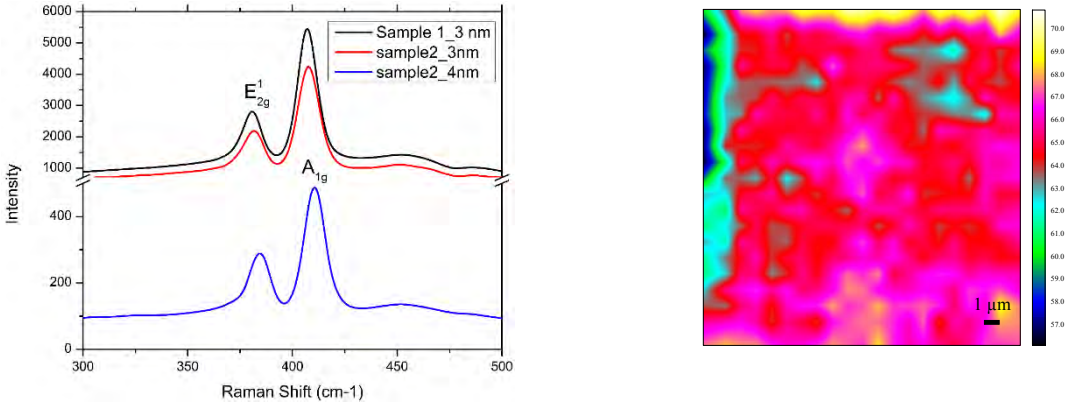

Figure 4. Typical Raman spectra of 3 nm and 4 nm MoS_2 films (left) and the representative Raman map of 3 nm film (right) showing some non-uniformity across the sample.

The peak separations are almost the same for the samples and there is some variation of peak intensity due to the different quality of MoS_2. N5 has developed a protocol to map the Raman spectra over a large area and the data are shown in Fig. 4. The growth process has been further optimized to improve the uniformity and Raman maps of those samples are shown in Fig. 5 not reported earlier.

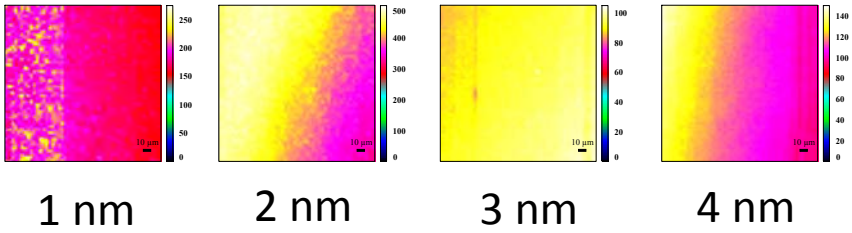

Figure 5. Raman maps (E_2 peak) of MoS_2 films grown on sapphire substrates showing no significant intensity variation across the sample that represents, good quality and uniformity over the mapped area of 400 μm^2.

In order to increase the drive currents, layer counts have been increased to 10 (over 6 nm thickness) which may increase the non-uniformity across the sample. Raman mapping has been implemented to measure the non-uniformity in these layers as. The graph in Fig. 6 compares the Raman spectra of 10 layer sample with a 3 layer sample and the higher intensity indicates (most likely) more uniform material.

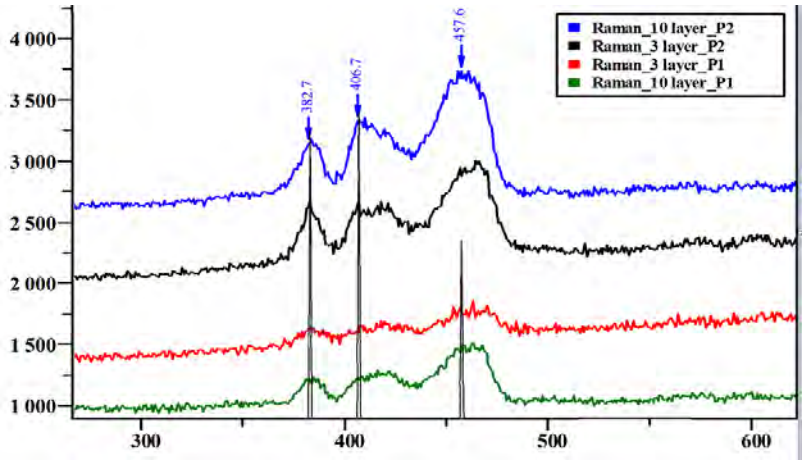

Figure 6. Comparison of Raman spectra between 10 and 3 layers of MoS_2.

Task 2: Development of Low-Resistance Source-Drain Contact Metallization Schemes and High-Performance Gate Dielectric

Subtask 2.1. Design and optimization of new source/drain metallization

N5 has developed the process flow for transistor fabrication along with the key processing tools (Fig. 7). N5's team has many years of experience in microfabrication. During the phase I of the project, N5 has optimized every single aspect of the fabrication process with emphasis on large-

scale manufacturing with high yield. N5 has further characterized the source and drain contacts, optimized etching of MoS2 for mesa fabrication (active channel formation), and gate oxide deposition using atomic layer deposition.

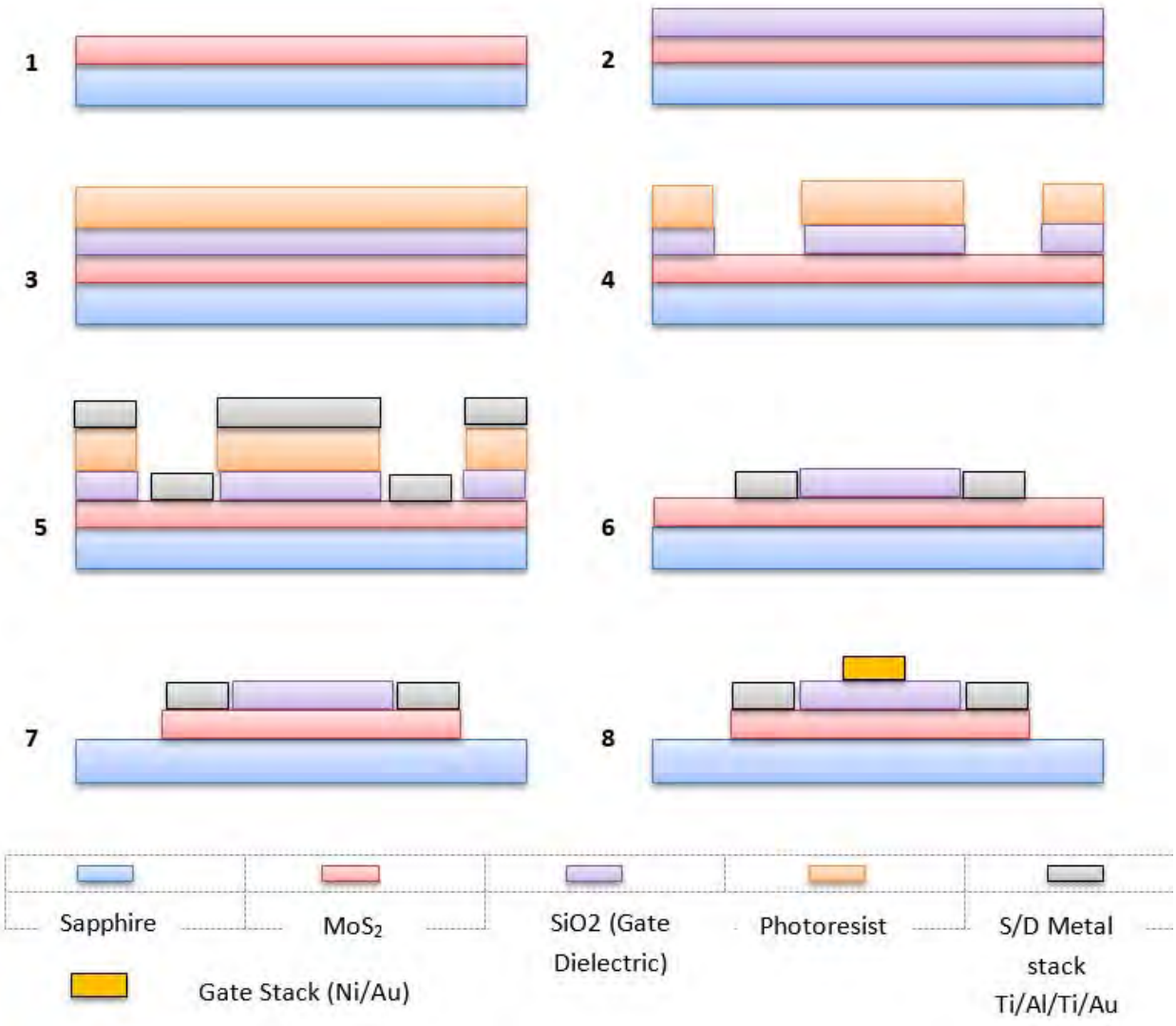

Figure 7. Process flow showing etched multilayer MoS_2 to make source/drain contacts.

The most effective way of characterizing an ohmic metallization scheme is to extract its specific contact resistance (ρ_c, a contact area independent parameter) and transfer length using Transmission Line Measurements (TLM). Typical TLM pattern along with current-voltage characteristics is shown in Fig. 8. N5 has developed a multi-layer ohmic metal stacks of Ti/Al/Ti/Au (30/100/30/30 nm) which have been annealed at 200 C for 1 hour. Using this metal scheme and TLM method (Fig. 8), very small specific contact resistance has been achieved (10^{-4} – 10^{-5} ohm.cm^2). Sheet carrier concetration and hall-mobilty on large-area MoS_2 (3 and 4 nm thickness) using conventional van-der pauw measurements have been extracted. The table below summarizes the data for a 3 nm MoS_2 film grown on Sapphire substrate:

Sheet Resistance	5270 Ω /sqaure
Sheet Carrier Cocentration (n-type from hall voltage sign)	2.1×10^{12} cm^{-2}
Hall mobility	10 cm^2 $V^{-1}s^{-1}$

Subtask 2.2. Design and optimization of gate dielectrics

Design and optimization of gate dielectric is very important for any FET. Utilizing high dielectric constant oxides (high k) one can increase the gate capacitance without decreasing the gate oxide thickness. N5 has used atomic layer deposition (ALD) method to deposit two gate dielectrics: one Al_2O_3 (k =11) and SiO_2 (k =3.9) as gate dielectrics. The deposition parameters of all these dielectrics has been varied to obtain a high quality interface to the 2D layer with low interface state density.

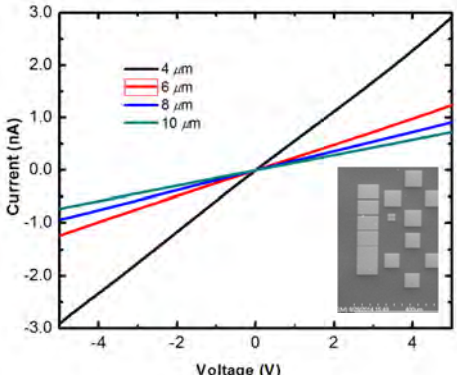

Figure 8. Linear current-voltage data between pads of different gaps of TLM pattern (inset).

Task 3. Design and Fabrication of 2D RF Transistor

In order to increase the drive currents, devices need to designed and fabricated with more layer of MoS_2. However, W/L ratios are also important consideration for drive current optimization. N5 has optimized the lithography process and Fig. 9 shows the scanning electron microscope image for devices with different W/L ratios with 50 nm Al_2O_3 as gate oxide.

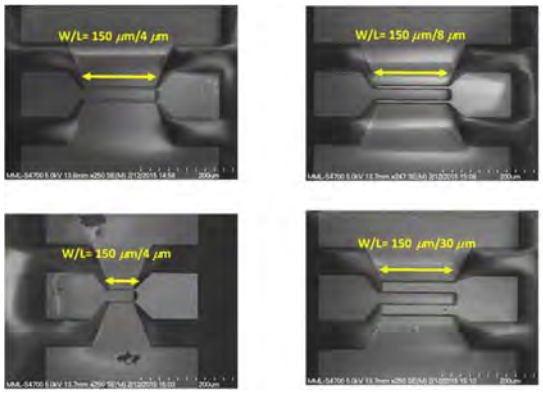

Figure 9 Fabricated 2D RF transistor with various W/L ratio.

Task 4. Measurement of RF Performance

In order to evaluate the performance, figures of merit of the fabricated RF transitors have been extracted. Transconductance of a transistor which measures the effectiveness of the gate signal to modulate the channel current has been extracted for various W/L ratios shown in Fig. 9. Typical transconductance plots of 4 nm MoS_2 devices (normalized drain current with gate dimensions) are shown in Fig. 10. Promising observations are that the normalized current and the transconductance are similar for various W/L ratios, which indicates uniformity. However, the transconductance values are still low and together with the fact that the devices in this particular batch showed a p-type behaviour (the reason for this not clear at this time). It was not clear the reason behind this unusual un-intentionl p-type behavior. If this could be understood and reproduced, there is a possibility of producing CMOS type circuits on the same film.

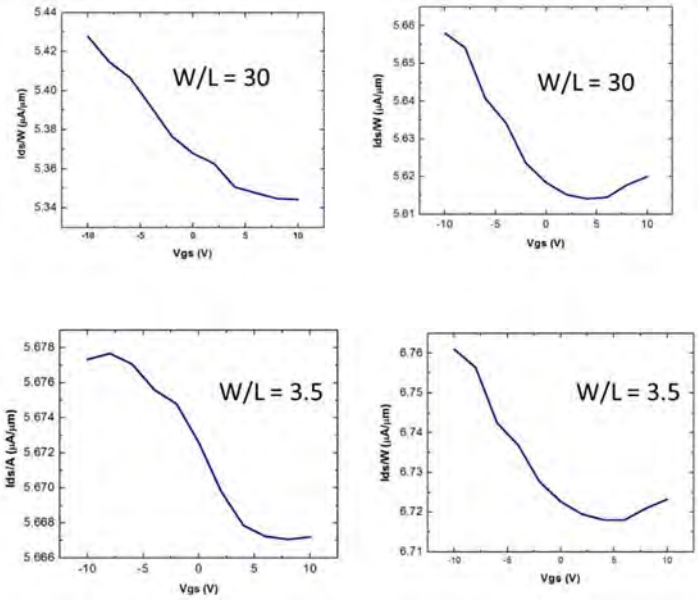

Figure 10 Transconductance of fabricated 2D RF transistor with various W/L ratio.

On the contrary, the transconductance plot of another MoS_2 (top-gated, Ni/Au) transistor (4 nm thickness) with ALD deposited SiO_2 gate dielectric shows the usual n-type behavior (Fig. 11). However, the top gate leakage is still 2 orders of magnitude smaller. The gate dielectric needs further optimization to improve the performance.

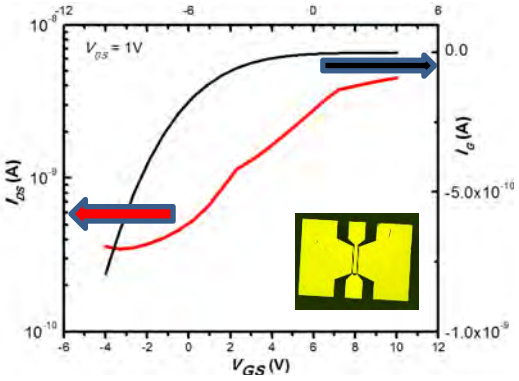

Figure 11. Transconductance of fabricated 2D RF transistor with various W/L ratio. Inset shows the actual device

DC characterics of further optmized fabricated transitor is shown in Fig. 12. The data show that the channel current decreases with reverse biasing the gate, signature of n-type channel material (typical of MoS_2 films). From

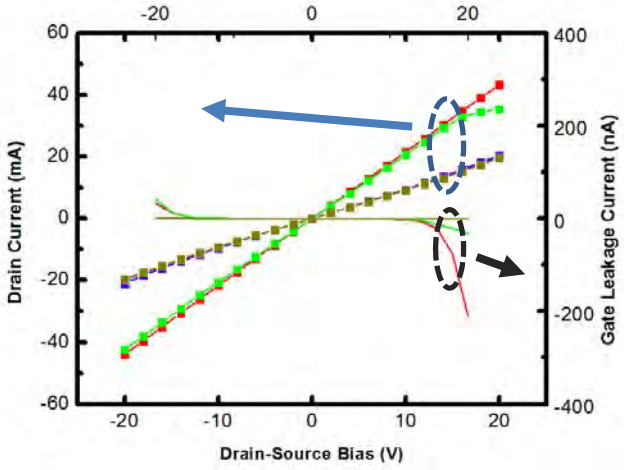

Figure 12. DC characteristics of RF transistor made with 4 nm MoS_2.

the graph above it is clear that gate leakage is 3 order of magnitude smaller than that channel current indicating decent gate performance. Although the normalized channel current is 0.13 mA/μm (high), the gate drive is poor and this is possibly realted to the low-mobilty measured in the samples.

N5 has developed a setup to measure the scattering parameter measurement on the RF transistors. The setup is shown in Fig. 13 in which HP 8510C 20 GHz VNA is connected to a probe station using semi-rigid RF cables to cascade RF probe manipulators. The Agilent B15000A is connected to the VNA through internal bias-Ts of the VNA, which provides the DC bias.

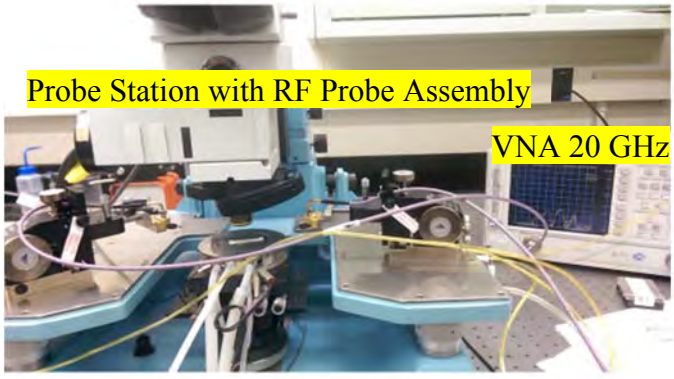

Figure 13. S parameters setup developed by N5.

Using this setup the S-parameters of the biased devices have been extracted. However the S_{12} and S_{21} parameters were in the range of -17 dB (at 0.5 GHz) which is physically un-realistic for a transistor as that would imply an insertion loss. However, we suspect that high contact resistances are still there along with poor gate drive. De-embedding method would be appropriate to extract the intrinsic parameters of the channel itself, excluding the parasitic drain and source resistances.

4. Technical Feasibility

During the STTR phase I, N5 focused on the large-area growth of mono and multi-layer MoS_2 layers using chemical vapor deposition methods with large-area uniformity and reproducibility for RF transistors. Feasibility of large-periphery RF device fabrication has been demonstrated using conventional methods that utilize either contact or projection lithography for high throughput device manufacturing. This further paves the way to transfer the growth process over 1 inch or 2 inch wafer for scalable device development. N5 has utilized multilayer strategies (i.e., higher layer count) rather than single layer which are more commercially viable for scaling up the growth process. Various processes such as metallization scheme, high k gate dielectric deposition has been standardized- an important step for device fabrication. Although unusual p-type behavior has been observed for few samples instead of usual n-type, it would be interesting to explore and investigate the mechanism for such characteristics in future.

Phase II Plans

1. Utilization of atomic layer deposition for large area deposition of 2D materials

GMU team has already started growing TD materials using atomic layer deposition technique. In phase II, N5 plans to utilize ALD deposited 2D materials for transistor development

2. Develop a robust manufacturing process to develop large area devices with high yield and reliability

N5 team has established feasibility of the manufacturing process for realizing realistic RF transistor geometries. For commercial applications, it is imperative to use batch manufacturing processes such as projection lithography and not electron-beam lithography.

3. Demonstrate transistors with significant gain and figures of merit improvement in GHz range operation

N5 team has done significant comparison of devices made from different layer thicknesses, the tradeoff are current drive capability, ability to form ohmic contacts with low-contact resistances, transconductance per gate length, and noise performance. Based on our phase I findings, we are confident that we can deliver a prototype device in phase II, that can be used for system level integration such as low-noise amplifier for low-power applications.